Electronic Version
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Adiabatic Charging Register Circuit

Abstract

An adiabatic charging register circuit comprising a plurality of n-channel MOSFET's and a plurality of p-channel MOSFET's, is operated by a clock signal which has a gradually rising and a gradually falling waveform generated by using a charge recycle power source in which charge supplied to a load is at least partially collected to said charge recycle power source, and following inequality is satisfied;

$$\left| V_{TN} \right| + \left| V_{TP} \right| \geq VDD$$

where V_{TN} is threshold of an n-channel MOSFET, V_{TP} is threshold of a p-channel MOSFET, and VDD is output voltage of said charge recycle power source.